REMARKS

The examiner has rejected claims 1-3, 5, 7-9 and 12-13 under 35 U.S.C. §103(a) as being unpatentable over the publication "A Parallel Pipelined DSP Processor Core" by Aikens et al. The examiner has objected to claims 4, 6, and 10-11 as being dependent upon a rejected base claim.

In response, applicant has amended claims 4, 6, and 10-11 to be in independent form including all of the limitations of the base claim and any intervening claims. Allowance of claims 4, 6, 10 and 11 as amended is respectfully requested.

The examiner states that

> "...Aiken [sic] et al. do not disclose the claimed 'combination phase computing element'; however the 'processing and communicating tree' (PCT) could provide the equivalent functions as claimed. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the invention as claimed according to Aiken [sic] et al's teaching because the reference discloses a parallel pipelined DSP processor for performing FFT."

THE AIKENS ET AL. PUBLICATION

Aikens et al., show a general purpose DSP (digital signal processor) core. The architecture of the DSP core contains parallel processing cells (PPC) followed by a binary tree structure (PCT), followed by a Multi-Function Generator. A DSP core is a general computing structure that may be programmed to perform different functions. Aikens et al. suggest that

the proposed DSP core could be used to implement several known signal processing applications, namely, 1) convolution, 2) discrete Fourier Transform and 3) discrete cosine transform.

Aikens et al. discuss using the DSP core to perform the discrete Fourier Transform function. There are various algorithms for computing the discrete Fourier Transform. Aikens et al. describe what Cooley-Tukey have proposed in their discovery (the binary tree), which is based on bit reversing technique as stipulated on the top of page 83 of the Aikens et al. publication.

DSP cores are designed to be very general machines in order to be useful across a wide variety of digital signal processing applications. Even if a DSP core "could provide" a given function, it does not follow that all the functions that a DSP "could provide" are therefore obvious to one of ordinary skill in the art. Only if the given function for which the DSP "could be" put to use is suggested or shown by the prior art, would the given function then be considered obvious. In other words, only those DSP functions that are shown or reasonable suggested by the prior art are rendered obvious.

CLAIM LANGUAGE DISTINGUISHES AIKENS ET AL.

Claim 1 recites a plurality of parallel processing elements

> "each of said plurality of r parallel processing elements being independent of each other and having at least two stages of butterfly computing elements"

Aikens et al., shows a parallel processing element with a single stage of butterfly processing elements. (Aikens et al. page 82, figure 2 and page 83, column 2).

Claim 1 also recites a combination phase, having a characteristic that,

> "said combination phase computing element including a single stage of butterfly computing elements"

The processing and communicating tree (PCT) is described by Aikens et al. as having a "binary tree structure" (Aikens et al. page 81). Whether or not a binary tree structure "could be" a "single stage of butterfly computing element" is not the issue. The issue is whether Aikens et al. show or suggest that the binary tree structure is programmed to be a "single stage of butterfly computing elements". Aikens et al. do not remotely suggest that that the binary tree structure is or should be programmed to be a "single stage of butterfly computing elements". Aikens et al. confine their entire discussion of butterfly computing elements to the parallel processing cells (PCC). Therefore it would not be obvious to one of ordinary skill in the art from a reading of Aikens et al. to program the PCT to be a "single stage of buttefly computing elements."

Similarly, for claim 12, Aikens et al. do not show "parallel processing elements being independent of each other and having at least two stages of butterfly computing elements" followed by a combination phase computing element having "a single stage of

butterfly computing elements". Claim 2-11 and 13 recite specific mathematics that facilitate the claimed architecture.

CONCLUSION

Applicant has amended claims 4, 6, 10 and 11 to be in independent form. Withdrawal of the examiner's objection to claims 4, 6, 10 and 11 as amended is solicited.

Applicant has made an earnest effort to show how the language of the claims distinguishes the prior art to Aikens et al. It is requested that the examiner withdraw the rejection under 35 U.S.C. §103(a) and pass the present application to issue.

Respectfully submitted,
by

DATED: Dec 4, 2003

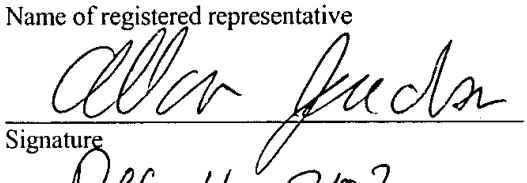
ALLAN J. JACOBSON
Attorney for applicant
Registration No. 29,079
13310 Summit Square Center
Langhorne, Pennsylvania 19047
telephone:(215) 579-1426

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on

Date: Dec 4 2003

ALLAN J. JACOBSON
Name of registered representative



Signature

Dec 4 2003

Date of signature